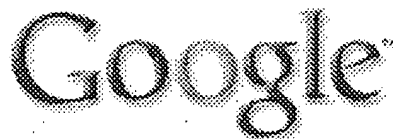


L Number	Hits	Search Text	DB	Time stamp
1	149	717/149.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 15:25
2	68	717/150.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 15:25
3	195	717/159.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 15:27
4	43	708/498.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 15:27
5	47	708/513.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 15:30
6	207	712/22.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 15:30
-	18	multiple with data with single adj1 register	USPAT	2004/03/18 13:42
-	27	multiple with data with single adj1 register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 13:47
-	11	parallel with data with single adj1 register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 13:48
-	12	((("6038652") or ("5958038") or ("5881259") or ("5692207") or ("5390135") or ("5381531") or ("5230057") or ("5907694") or ("5847978") or ("5818364") or ("5689450") or ("5669010"))).PN.	USPAT	2004/03/19 13:51
-	5	((("5594679") or ("5418915") or ("5408670") or ("5218564") or ("4752873"))).PN.	USPAT	2004/03/19 13:52
-	8	"3257579"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/19 13:58
-	1	1996-331277.NRAN.	DERWENT	2004/03/19 13:56
-	1	"multisequencing a single instruction stream"	IBM_TDB	2004/03/19 13:59
-	131	"single instruction stream"	IBM_TDB	2004/03/19 14:02
-	1	"high speed parallel signature board"	IBM_TDB	2004/03/19 15:25


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ah al ax register

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**[PDF] AH AL AX**File Format: PDF/Adobe Acrobat - [View as HTML](#)... well. 15 8 7 0 **AH AL AX** Page 2. ... stack. In fact, all references to memory on the IBM PC involve a segment **register** as a base location. ...[www.math.uaa.alaska.edu/~afkjm/cs221/handouts/irvine2.pdf](http://www.math.uaa.alaska.edu/~afkjm/cs221/handouts/irvine2.pdf) - [Similar pages](#)**[PDF] Lecture 9 INC and DEC INC/DEC Examples ADD**File Format: PDF/Adobe Acrobat - [View as HTML](#)... Format: DIV divisor divisor - **register** or memory (not immediate!) • **Registers** used: Dividend Divisor Quotient Remainder **AX** op-8 **AL AH** DX:**AX** op-16 **AX** DX ...[www.cs.wpi.edu/~jburge/courses/c02/cs2011/lectures/Lecture9.PDF](http://www.cs.wpi.edu/~jburge/courses/c02/cs2011/lectures/Lecture9.PDF) - [Similar pages](#)**[PDF] Memory Addressing and Registers Memory Addressing and Registers ...**File Format: PDF/Adobe Acrobat - [View as HTML](#)... **AX AX** Spring 2001 CA103 Computer Architecture Ray Walshe Page 2 Memory Addressing and **Registers** - In the previous example • **AH** contains D7 and **AL** contains ...[www.computing.dcu.ie/~ray/NewCA103/Addressing.pdf](http://www.computing.dcu.ie/~ray/NewCA103/Addressing.pdf) - [Similar pages](#)**SAVING AND RESTORING VGA SCREENS by Ben Myers [LISTING ONE] PAGE ...**... **ax** ; restore default Enable Set/Reset **register** mov dx,3C4h ; DX = Sequencer I/O port ; **AH** = all planes enabled mov ax,0F02h ; **AL** = Map Mask **Register** number (2 ...[www.ddj.com/ftp/1991/1991.07/vga.asc](http://www.ddj.com/ftp/1991/1991.07/vga.asc) - 19k - [Cached](#) - [Similar pages](#)**Use of IMUL demonstration**... 0FFh (255) in **ax** MOV **AL**,1 ; put +1 into **al** MOV **AH**, -1 ; put -1 into **ah** IMUL **AH** ; signed mul ... **BX** ; signed mul - result of FFFF:FFFF in dx:ax - correct ; \*\*\*\* dword ...[www.jorgon.freemove.co.uk/TestbugHelp/UseofIMUL.htm](http://www.jorgon.freemove.co.uk/TestbugHelp/UseofIMUL.htm) - 6k - [Cached](#) - [Similar pages](#)**Disassembly of "Bad Street Brawler" loader**... far start: mov **ah**,0Fh int 10h ; Video display **ah**=functn 0Fh ; get state, **al**=mode, **bh**=page ; **ah**=columns on screen push **ax** xor **ah**,**ah** ; Zero **register** mov **al**,5 int ...[www.oldschool.org/shrines/lbd/examples/header.html](http://www.oldschool.org/shrines/lbd/examples/header.html) - 5k - [Cached](#) - [Similar pages](#)**Copyright (C) 2002 - Alexander Popov ; <a href="http://www.emu8086 ...**... MOV **AL**, char MOV **AH**, 0Eh INT 10h POP **AX** ENDM ; This procedure gets the multi-digit ; SIGNED number from the keyboard, ; and stores the result in **CX register**: ...[www.emu8086.com/vb/asm\\_samples/ToBin.txt](http://www.emu8086.com/vb/asm_samples/ToBin.txt) - 7k - [Cached](#) - [Similar pages](#)**"Extended Cursor Handling unit" by CHAD MOORE**... offset } MOV **DX**,03D4H { CRTC index **register** } MOV **AL**,0EH { select **register** 0EH } OUT **DX**,**AL** INC **DX** { CRTC data **register** } IN **AL**,**DX** SHL **AX**,08H { **AH** = high bits ...[www.bsdc.org/swag/CURSOR/0032.PAS.html](http://www.bsdc.org/swag/CURSOR/0032.PAS.html) - 22k - [Cached](#) - [Similar pages](#)**My Assembler Tutorials**... their parameters. Each instruction takes only one parameter and the other is always the **AX** (and/or **AL** and **AH**) **register**. Here are ...[www.csn.ul.ie/~darkstar/assembler/tut5.html](http://www.csn.ul.ie/~darkstar/assembler/tut5.html) - 9k - [Cached](#) - [Similar pages](#)**[PDF] Arithmetic Instruction**File Format: PDF/Adobe Acrobat - [View as HTML](#)... or memory **AL AH** word / word **AX** = word, **DX** = 0 **Register** or memory **AX** **DX** word / byte


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### X-bit labs - Articles - SSE Technology in New Intel Prescott ...

... The CPU cannot place different data to be processed similarly in a **single register**. ... hard thing, although most effective; the use of a **SIMD compiler**, which may ...

[www.xbitlabs.com/articles/cpu/display/prescott-sse\\_2.html](http://www.xbitlabs.com/articles/cpu/display/prescott-sse_2.html) - 53k - [Cached](#) - [Similar pages](#)

### Gamasutra - Features - Wyatt's World - "Cracking Open The Pentium ...

... **Single register** indirect addressing is the only addressing mode ... contains macros for all the **SIMD** instructions and ... Visual C++ and the Intel **compiler** know what ...

[www.gamasutra.com/features/wyatts\\_world/19990528/pentium3\\_05.htm](http://www.gamasutra.com/features/wyatts_world/19990528/pentium3_05.htm) - 47k - [Cached](#) - [Similar pages](#)

### Optimizations of loop induction variables though **SIMD** instructions

... more quickly than four), but by packing multiple values into a **single register** it also ... **Compiler** Vectorization Techniques for a Disjoint **SIMD** Architecture. ...

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### [PS] Compiling For **SIMD** Within A Register

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... allows this rearrangement within a **single register** (thus not ... 3 **Compiler** Optimizations For SWAR Optimizations that have been devised for **SIMD** programming often ...

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... allows this rearrangement within a **single register** (thus not ... 3. **Compiler** Optimizations For SWAR Optimizations that have been devised for **SIMD** programming often ...

[www.phys.aoyama.ac.jp/~aoyama+/Tech\\_notes/adaptor\\_doc/Users\\_Guide.pdf](http://www.phys.aoyama.ac.jp/~aoyama+/Tech_notes/adaptor_doc/Users_Guide.pdf) - [Similar pages](#)

### [PDF] **AC Compiler** for a Processor with a Reconfigurable Functional Unit

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... operation with multiple register inputs and a **single register** output. The goal of the **c mpiler** is to identify the ... The second step is the **SIMD** Within A Register ...

[www.ee.washington.edu/faculty/hauck/publications/compiler.PDF](http://www.ee.washington.edu/faculty/hauck/publications/compiler.PDF) - [Similar pages](#)

### ILP

... required to support a **single register** file severely ... ameliorated by using advanced **compiler** loop optimization ... accurate modeling of vector (**SIMD**) operations and ...

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### [PDF] Novel Multimedia Instruction Capabilities in VLIW Media Processors

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... SuperOperations in Hardware **single register** file **single register** file FU-5 FU-5 ... (as all other multimedia and **SIMD** operations) • The **C compiler** maps these ...

[www.hotchips.org/archive/hc10/hc10pres\\_pdf\\_1up/hc98\\_8b\\_eijndhoven\\_1up.pdf](http://www.hotchips.org/archive/hc10/hc10pres_pdf_1up/hc98_8b_eijndhoven_1up.pdf) - [Similar pages](#)

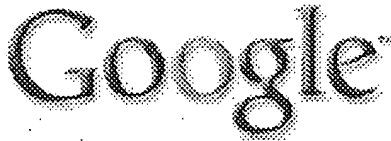
### [PDF] Register Organization and Raw Hardware 1 Register Organization for ...

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... The area of a **single register** cell is proportional to (p ... times as many registers as a **SIMD** register file ... The **compiler** for StreamIt, the pro- gramming language ...

[cva.stanford.edu/ee482s/scribed/lect07.pdf](http://cva.stanford.edu/ee482s/scribed/lect07.pdf) - [Similar pages](#)

### Bitwidth aware global register allocation

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### About SIMD

... **What is SIMD?** ... A SIMD system packs multiple data elements into a **single register** and performs the same calculation on all of them at the same time. ...

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... Page 6. **What is SIMD?** ... A SIMD system packs multiple data elements into a **single register** and performs the same calculation on all of them at the same time. ...

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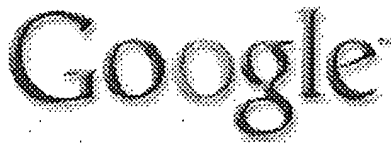
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**Web Definition:** **SIMD** - Single instruction stream-multiple data stream machine. A parallel processing system consisting of a set of n processors, n memories, an interconnection network and a control unit. The control unit broadcasts instructions to the processors and all active processors execute the same instruction at the same time.

[nivel.euitto.upm.es/tele/AYU/Dic/GLOS/GLOSS.HTM](http://nivel.euitto.upm.es/tele/AYU/Dic/GLOS/GLOSS.HTM) - [More definitions](#)

### Googlism what is simd

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[www.googlism.com/what\\_is/s/simd/](http://www.googlism.com/what_is/s/simd/) - 16k - Supplemental Result - [Cached](#) - [Similar pages](#)

### What is... SIMD (a definition)

SIMD (Single Instruction Multiple Data). As one of the three performance enhancements of MMX, SIMD lets one microinstruction operate ...

[iroi.seu.edu.cn/books/ee\\_dic/whatis/simd.htm](http://iroi.seu.edu.cn/books/ee_dic/whatis/simd.htm) - 4k - [Cached](#) - [Similar pages](#)

### About SIMD

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... mechanisms: SIMD execution and sub- word parallelism • a short-vector memory architecture • a two-cycle-deep computational pipeline **What is SIMD** parallelism ...

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### SIMD Panel Report

... parallel system. \$ Image Understanding Architecture, designed for integrated real-time vision tasks. 2. **What is SIMD?** The first ...

[www.ece.ucsb.edu/Faculty/Parhami/pubs\\_folder/f13\\_simd\\_panel.htm](http://www.ece.ucsb.edu/Faculty/Parhami/pubs_folder/f13_simd_panel.htm) - 41k - [Cached](#) - [Similar pages](#)

### Review Questions for Module4: Multimedia Operating Systems and ...

... How do you increase hit rate? Parallelism. **What is SIMD** and MIMD? How does it affect the performance? Back to Multimedia Architectures.

[vsp2.ecs.umass.edu/dvd/module4/questions.html](http://vsp2.ecs.umass.edu/dvd/module4/questions.html) - 2k - [Cached](#) - [Similar pages](#)

### Into The Fray With SIMD

... **What Is SIMD?** Single Instruction, Multiple Data (SIMD) processors are also known as short vector processors. They enable a single ...

[www.cs.umd.edu/class/fall2001/cmsc411/projects/SIMDproj/project.html](http://www.cs.umd.edu/class/fall2001/cmsc411/projects/SIMDproj/project.html) - 32k - [Cached](#) - [Similar pages](#)

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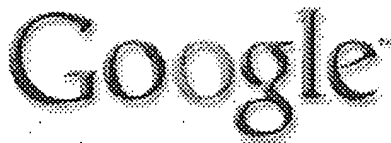
... **What is "SIMD"?** 4. Needless to say, the paper in its current form is not ready for publication. I can suggest several things that need to be done. ...

[bmrc.berkeley.edu/courseware/cs294/fall97/admin/grades/gna](http://bmrc.berkeley.edu/courseware/cs294/fall97/admin/grades/gna) - 5k - [Cached](#) - [Similar pages](#)

### The Hardware Site. Intel MMX Technology FAQ'S

... Go up. **What is SIMD ?** SIMD stands for Single Instruction, Multiple Data. This means that a single instruction operates on multiple pieces of data in parallel. ...

[www.hardwarepage.nl/mmxfaq.html](http://www.hardwarepage.nl/mmxfaq.html) - 10k - [Cached](#) - [Similar pages](#)


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### Automatic intra-register vectorization for the Intel architecture

... RJ Fisher and HG Dietz, Compiling for **SIMD within a Register**, 1998 Workshop on Languages and Compilers for Parallel Computing, University of North Carolina at ...

portal.acm.org/ citation.cfm?id=586555&dl=ACM&coll=portal&CFID=11111111&CFTOKEN=222222 - [Similar pages](#)

### [PDF] Numerisch Paralleles Rechnen

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Page 1. Dr. Peter Arbenz Oscar Chinellato Numerisch Paralleles Rechnen Assignment 3: **SIMD Within A Register** (SWAR) Ausgabe: 7.11.2002 Abgabe: 14.11.2002 In this ...

www.wr.inf.ethz.ch/education/pr/files/u3/u3.pdf - [Similar pages](#)

### Corinna G. Lee's Research on Vector Microprocessors

... Andrea Olgiati, Stuart V. Quick and John W. Lumley. Hewlett-Packard Labs, Bristol UK. Compilation for SWAR (**SIMD Within a Register**) Processors, 1997. ...

www.eecg.toronto.edu/~corinna/vector/related/ - 8k - [Cached](#) - [Similar pages](#)

### Corinna G. Lee's Research on Vector Microprocessors

... Compilation for SWAR (**SIMD Within a Register**) Processors, Purdue University, 1997. NESL: A Parallel Programming Language, Carnegie Mellon University, 1994-96. ...

www.eecg.toronto.edu/~corinna/vector/ - 9k - [Cached](#) - [Similar pages](#)

### [PDF] AC Compiler for a Processor with a Reconfigurable Functional Unit

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... instructions to put into the RFU. The second one is **SIMD Within A Register** (SWAR) optimization. The SWAR concept divides a register ...

www.ee.washington.edu/faculty/hauck/ publications/compiler.PDF - [Similar pages](#)

### [PDF] AC Compiler for a Processor with a Reconfigurable Functional Unit

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... sequence: control localization. Next, we describe the application of the RFU to **SIMD Within A Register** (SWAR) operations. Lastly, we ...

www.ece.northwestern.edu/cpdc/ Match/Pubs/fpga2000.ye.pdf - [Similar pages](#)

### [PDF] An Extended C Language and A SIMD Compiler for Efficient...

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... One preferable pre- vious research is a SIMD Compiler experimentally de- veloped for compiling the **SIMD Within A Register** C (SWARC)[5], a data parallel C ...

www.ph.tn.tudelft.nl/~wcaaris/ smartcarr/files/1dc-mmx.pdf - [Similar pages](#)

### [PPT] Lecture 1

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... Instruction combining. Control localization. **SIMD Within a Register**. Simulation Studies. Example applications only require 8 RFUOPs in the reconfigurable array. ...

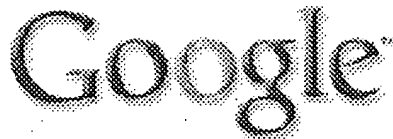
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... Page 12. 3/18/2003 Lecture 18 CHIMERA • Programmed in C – Instruction combining – Control localization – **SIMD Within a Regist r** • Simulation Studies ...

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### Linux Parallel Processing HOWTO: SIMD Within A Register (eg. using ...

... bit, and some machines only provide **signed** shift right ... Thinking Machines

CM1/CM2/CM200

**SIMD** supercomputers was ... it is probably best to develop **SWAR** algorithms as ...yara.ecn.purdue.edu/~pplinux/PPHOWTO/pphowto-4.html - 26k - Mar 17, 2004 - [Cached](#)- [Similar pages](#)

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### [PS] Compiling for for SIMD Within A Register

File Format: Adobe PostScript - [View as Text](#)... Mul X Mul by Sign (-,0,+) X Mul/Add X Average X Shift Left/Right XX X **Signed** ShiftRight ... **SIMD** isn't dead ... **SWAR** is a commercially important class of parallel. ...min.ecn.purdue.edu/~rfisher/Research/LCPC98/slides.ps - [Similar pages](#)

### [PS] The Scc Compiler: SWARing at MMX and 3DNow!

File Format: Adobe PostScript - [View as Text](#)... and loops modified to incorporate **SIMD** enable masking. ... Hardware **SWAR** instructionsused to optimize emulation when ... Emulation Example: 2 bit **signed** saturated ADD. ...min.ecn.purdue.edu/~rfisher/Research/LCPC99/slides.ps - [Similar pages](#)[ [More results from min.ecn.purdue.edu](#) ]

### [PS] Compiling For SIMD Within A Register

File Format: Adobe PostScript - [View as Text](#)... Mixed **signed** and unsigned operands yield a **signed** result. ... ix, DEC, HP, Intel, MIPS,Motorola, and Sun have proven that hardware support for **SWAR**, **SIMD** Within A ...shay.ecn.purdue.edu/~swar/lcpc98.ps - [Similar pages](#)

### [PDF] 1 ParAlign: a parallel sequence alignment algorithm for rapid and ...

File Format: PDF/Adobe Acrobat - [View as HTML](#)... in the form of microparallelism or **SIMD** Within A Register (**SWAR**). ... to perform thisoperation using the **SIMD** technology has ... Z to e i-1, the **signed** and saturated ...www.techfak.uni-bielefeld.de/~nniemann/lectures/spdv/paper/rognes.pdf - [Similar pages](#)

### [PDF] Institutionen f or systemtechnik Department of Electrical ...

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... The well-known extension MMX, 3DNow! and AltiVec are all examples of the special

**SIMD** technique **SWAR**, which will be further discussed in Section 3.8. ...www.isy.liu.se/cvl/ScOut/Masters/Papers/Ex3088.pdf - [Similar pages](#)

### From: Hank Dietz <pplinux@ecn.purdue.edu> Newsgroups: comp.os. ...

... Processing-HOWTO/part1 Last-modified: 5 Jan 98 -----BEGIN PGP SIGNED MESSAGE-----

The ... in the future, it may mean "Slot 2".... **SWAR**: **SWAR** (**SIMD** Within A ...faq5.jmas.co.jp/FAQs/linux/howto/ Parallel-Processing-HOWTO/part1 - 78k - [Cached](#) - [Similar pages](#)

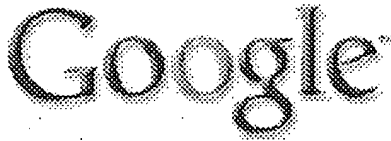
### From: Hank Dietz <pplinux@ecn.purdue.edu> Newsgroups: comp.os. ...

... HOWTO/part3 Last-modified: 5 Jan 98 -----BEGIN PGP SIGNED MESSAGE----- The ... 4.2.

Introduction To **SWAR** Programming The basic concept of **SWAR**, **SIMD** Within A ...faq5.jmas.co.jp/FAQs/linux/howto/ Parallel-Processing-HOWTO/part3 - 56k - [Cached](#) - [Similar pages](#)

### yellowdog-general: AltiVec and Open Source

... AC like language for dealing with **SIMD** instructions across ... <http://shay.ecn.purdue.edu/~swar/Swarc/Index> ... vector unsigned char) vec\_sums((vector **signed** long) work ...


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swar "sign bit" signed simd

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### Linux Parallel Processing HOWTO: SIMD Within A Register (eg. using ...

... nearest neighbor communication for **SWAR** using unpartitioned ... if shifts right preserve

the **sign bit**, and some machines only provide **signed** shift right. ...

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[PS] [Linux Parallel Processing HOWTO Hank Dietz](#)

[pplinux@ecn.purdue.edu ...](#)

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... **SWAR (SIMD Within A Register)** is a generic term for the concept of partitioning a register into multiple integer fields and using register-width operations to ...

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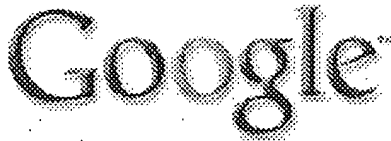
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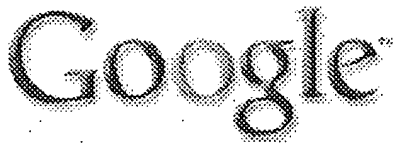
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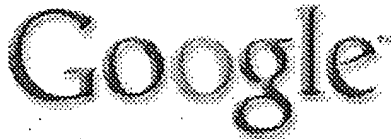
... Also, RAM and **SWAR** were applied to all sections in the absence of primary antibodies. These controls gave **negative** test results on all biopsy specimens used in ... [www.blackwell-synergy.com/links/doi/10.1046/j.1523-1755.2001.00019.x/full/](http://www.blackwell-synergy.com/links/doi/10.1046/j.1523-1755.2001.00019.x/full/) - [Similar pages](#)

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 ... XPL-9 49 721.5 1131.1 **Negative** Xpl-17 5 5.0 119.6 **Negative** • The number of ... Mud spring Big spr ing Salvador a Lower U runendes spring **Swar** tmodder Salvador a ... [www.predatorconservation.com/library/kunene%20lion%20reports/may%202001%20report.pdf](http://www.predatorconservation.com/library/kunene%20lion%20reports/may%202001%20report.pdf) - [Similar pages](#)

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&gt; Glad to see the Altivec patches have made it into the tree. ...

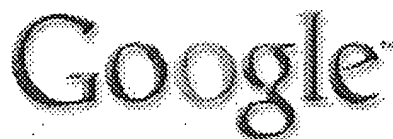
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